In the Claims:

1.   (Previously Amended.) A test circuit, provided between first and second target circuits, for testing the target circuits, comprising:

a first selecting section for selecting and outputting one of three input signals, namely: (1) a first output signal output from the first target circuit, (2) a second output signal output from the second target circuit, and (3) a test signal indicating a test pattern input via a test pattern input terminal, said selection being made according to first and second test mode signals supplied to said first selecting section as additional inputs used for selection, said first and second test mode signals supplied from an external device;

a temporary data storage section for temporarily storing the signal selected by the first selecting section as a data signal;

a second selecting section for selecting, as a first selection signal. one of the temporarily stored data signal or the second output signal from the second target circuit according to the second test mode signal, and providing the first selected signal to the first target circuit; and

a third selecting section for selecting, as a second selecting signal, one of the temporarily stored data signal or the first output signal from the first target circuit according to a third test mode signal supplied from said external device, and providing the second selected signal to the second target circuit, and wherein:

the temporarily stored data signal is also output as a test result via a test pattern output terminal.

2.   (Original)   An integrated circuit device including a test circuit as claimed in claim 1.

3.   (Original)   A test circuit as claimed in claim 1, wherein the first, second, and third selecting sections are multiplexers.

4.   (Withdrawn)   A system of forming test circuits for testing target circuits in an, integrated circuit device, comprising:

a parallel number calculating section for calculating the number of input-output chains, each chain for inputting and outputting a test signal, based on the number of test terminals for connecting the integrated circuit device and external circuits;

a detecting section for comparing the number of input terminals and the number of output terminals of each target circuit, and determining a larger or equal number as a compared result; and

a serial length calculating section for calculating a serial length for the relevant target circuit by dividing the number determined by the detecting section by the parallel number calculated by the parallel number calculating section, where the serial length indicates the number of storage elements which are serially connected, and

wherein the number of input-output chains for parallel-testing each target circuit is determined based on the parallel number calculated by the parallel number calculating section, and the serial length of each input-output chain is determined based on the serial length for the relevant target circuit calculated by the serial length calculating section.

5.   (Withdrawn)   A system of forming test circuits for testing target circuits in an integrated circuit device, comprising:

a parallel number calculating section for calculating the number of input-output chains, each chain for inputting and outputting a test signal, based on the number of test terminals for connecting the integrated circuit device and external circuits;

a detecting section for comparing each number of input terminals and each number of output terminals of the target circuits, and detecting a maximum number as a compared result; and

a common serial length calculating section for calculating a common serial length for all the target circuits by dividing the number determined by the detecting section by the

parallel number calculated by the parallel number calculating section, where the serial length indicates the number of storage elements which are serially connected, and

wherein the number of input-output chains for parallel-testing each target circuit is determined based on the parallel number calculated by the parallel number calculating section, and the serial length of each input-output chain is determined based on the common serial length calculated by the common serial length calculating section.

6.   (Withdrawn)   A system of forming test circuits for testing an integrated circuit device, comprising:

a test circuit forming section for forming test circuits as claimed in claim 1, where the number of the test circuits agrees with the number of pairs of input and output terminals of the first target circuit;

a core connecting section for connecting each test circuit formed by the test circuit forming section to a pair of input and output terminals of the first target circuit; and

a serial-connecting section for connecting an external terminal of the integrated circuit device and the test pattern input terminal of one of the test circuits, and repeating an operation of connecting the test pattern output terminal of the connected test circuit and the test pattern input terminal of another test circuit, so as to form a serial chain of a predetermined number of the test circuits, wherein:

a test result is output from the test pattern output terminal of the last connected test circuit.

7.   (Withdrawn)   A system of forming test circuits, as claimed in claim 6, further comprising:

a parallel-connecting section for providing separated serial chains, based on the number of test terminals for connecting the integrated circuit device and external circuits, and the number of the pairs of input and output terminals, and

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wherein a test signal is supplied to each serial chain provided by the parallel-connecting section, and a test result is output from the test pattern output terminal of the last connected test circuit of the relevant chain.

8.   (Currently Amended) An integrated circuit device including a target circuit to be tested, and a test circuit as recited in claim 1 comprising:

a plurality of test circuits as claimed in claim 1, where the number of the test circuits agrees with the number of pairs of input and output terminals of the first target circuit, wherein:

each test circuit is connected to a pair of input and output terminals of the first target circuit;

an external terminal of the integrated circuit device is connected to the test pattern input terminal of one of the test circuits,

a serial chain of a predetermined number of the test circuits is formed by connecting an external terminal of the integrated circuit device and the test pattern input terminal of one of the test circuits, and repeating an operation of connecting the test pattern output terminal of the connected test circuit and the test pattern input terminal of another test circuit, and

the test pattern output terminal of the last connected test circuit is connected to another external terminal of the integrated circuit device for outputting a test result.

9.   (Previously Amended)   A test method of testing first and second target circuits, comprising the steps of:

selecting and outputting one of three input signals, namely: (1) a first output signal output from the first target circuit, (2) a second output signal output from the second target circuit, and (3) a test signal indicating a test pattern input via a test pattern input terminal, said selection being made according to first and second test mode signals supplied as additional inputs used in selection, said first and second test mode signals supplied from an external device;

temporarily storing the selected signal as a data signal;

selecting as a first selected signal, one of the temporarily stored data signal or the second output signal from the second target circuit according to the second test mode signal, and providing the first selected signal to the first target circuit;

selecting as the second selected signal, one of the temporarily stored data signal or the first output signal from the first target circuit according to a third test mode signal supplied from said external device, and providing the second selected signal to the second target circuit; and

outputting the temporarily stored data signal as a test result via a test pattern output terminal.

10. (Withdrawn)   A method of forming test circuits for testing target circuits in an integrated circuit device, comprising:

a parallel number calculating step of calculating the number of input-output chains, each chain for inputting and outputting a test signal, based on the number of test terminals for connecting the integrated circuit device and external circuits;

a detecting step of comparing the number of input terminals and the number of output terminals of each target circuit, and determining a larger or equal number as a compared result;

a serial length calculating step of calculating a serial length for the relevant target circuit by dividing the number determined in the detecting step by the parallel number calculated in the parallel number calculating step, where the serial length indicates the number of storage elements which are serially connected; and

a test chain determination step of determining the number of input-output chains for parallel-testing each target circuit based on the parallel number calculated in the parallel number calculating step, and determining the serial length of each input-output chain based

on the serial length for the relevant target circuit calculated in the serial length calculating step.

11.   (Withdrawn)   A method of forming test circuits for testing target circuits in an integrated circuit device, comprising:

a parallel number calculating step of calculating the number of input-output chains, each chain for inputting and outputting a test signal, based on the number of test terminals for connecting the integrated circuit device and external circuits;

a detecting step of comparing each number of input terminals and each number of output terminals of the target circuits, and detecting a maximum number as a compared result;

a common serial length calculating step of calculating a common serial length for all the target circuits by dividing the number determined in the detecting step by the parallel number calculated in the parallel number calculating step, where the serial length indicates the number of storage elements which are serially connected; and

a test chain determination step of determining the number of input-output chains for parallel-testing each target circuit based on the parallel number calculated in the parallel number calculating step, and determining the serial length of each input-output chain based on the common serial length calculated in the common serial length calculating step.

12.   (Withdrawn) A computer readable storage medium storing a program for making a computer execute an operation of forming test circuits for testing an integrated circuit device, the operation comprising:

a test circuit forming step of forming test circuits as claimed in claim 1, where the number of the test circuits agrees with the number of pairs of input and output terminals of the first target circuit;

a core connecting step of connecting each test circuit formed in the test circuit forming step to a pair of input and output terminals of the first target circuit;

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a serial-connecting step of connecting an external terminal of the integrated circuit device and the test pattern input terminal of one of the test circuits, and repeating an operation of connecting the test pattern output terminal of the connected test circuit and the test pattern input terminal of another test circuit, so as to form a serial chain of a predetermined number of the test circuits; and

a test result outputting step of outputting a test result from the test pattern output terminal of the last connected test circuit.

13.   (Withdrawn)   A computer readable storage medium as claimed in claim 12, the operation of the program further comprising:

a parallel-connecting step of providing separated serial chains, based on the number of test terminals for connecting the integrated circuit device and external circuits, and the number of the pairs of input and output terminals;

a test signal supplying step of supplying a test signal to each serial chain provided in the parallel-connecting step; and

a test result outputting step of outputting a test result from the test pattern output terminal of the last connected test circuit of the relevant chain.

14.   (Withdrawn)   A computer readable storage medium storing a program for making a computer execute an operation of forming test circuits for testing target circuits in an integrated circuit device, the operation comprising:

a parallel number calculating step of calculating the number of input-output chains, each chain for inputting and outputting a test signal, based on the number of test terminals for connecting the integrated circuit device and external circuits;

a detecting step of comparing the number of input terminals and the number of output terminals of each target circuit, and determining a larger or equal number as a compared result;

a serial length calculating step of calculating a serial length for the relevant target circuit by dividing the number determined in the detecting step by the parallel number calculated in the parallel number calculating step, where the serial length indicates the number of storage elements which are serially connected; and

a test chain determination step of determining the number of input-output chains for parallel-testing each target circuit based on the parallel number calculated in the parallel number calculating step, and determining the serial length of each input-output chain based on the serial length for the relevant target circuit calculated in the serial length calculating step.

15. (Withdrawn) A computer readable storage medium storing a program for making a computer execute an operation of forming test circuits for testing target circuits in an integrated circuit device, the operation comprising:

a parallel number calculating step of calculating the number of input-output chains, each chain for inputting and outputting a test signal, based on the number of test terminals for connecting the integrated circuit device and external circuits;

a detecting step of comparing each number of input terminals and each number of output terminals of the target circuits, and detecting a maximum number as a compared result;

a common serial length calculating step of calculating a common serial length for all the target circuits by dividing the number determined in the detecting step by the parallel number calculated in the parallel number calculating step, where the serial length indicates the number of storage elements which are serially connected; and

a test chain determination step of determining the number of input-output chains for parallel-testing each target circuit based on the parallel number calculated in the parallel number calculating step, and determining the serial length of each input-output chain based on the common serial length calculated in the common serial length calculating step.